Application Note

NOVOSENSE

Design Guide for NSD1224LA

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ABSTRACT

NSD1224LA is a high reliability low side-high side gate driver with two independent input pins HI and LI dedicated to be used in AC-DC and DC-AC power applications. Driver inputs are compatible with CMOS and TTL logic hence it provides easy interface with analog and digital controllers. The chip can deliver 3A peak source and -4A peak sink current to driver MOSFET and IGBT. Additionally, the interlock function is involved, the function can prevent the MOS/IGBT bridge from shooting through due to the driver inputs are high at the same time, which triggered by high-noise interference or other error MCU instructions.

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1.Applications and Implementation

1.1.Typical Applications

The circuit shows a typical half-bridge configuration by using the driver NSD1224LA which could be used in several popular power converter topologies such as half-bridge/full bridge/LLC isolated topologies applications.

NSD1224LA gate drivers offer high voltage (100 V), small delays (23 ns), and good driving capability (+3A，-4A) in a single device. The floating high-side driver is capable of operating with switch node voltages up to 100 V. This allows for N-channel MOSFETs control in half-bridge, full-bridge, synchronous buck, synchronous boost, and active clamp topologies. NSD1224-LA gate driver IC also has built-in bootstrap diode to help power supply designers optimize PWB area and to help reduce bill of material cost in most applications. The driver (DFN10 package) has an enable/disable functionality to be used in applications where driver needs to be enabled or disabled based on fault condition in other parts of the circuit. Interlock functionality of the device is very useful in applications where overall reliability of the system is of utmost criteria and redundant protection is desired.

For NSD1224LA, each channel is controlled by its respective input pins (HI and LI), allowing flexibility to control ON and OFF state of the output. Both the outputs are forced OFF when the two inputs overlap.

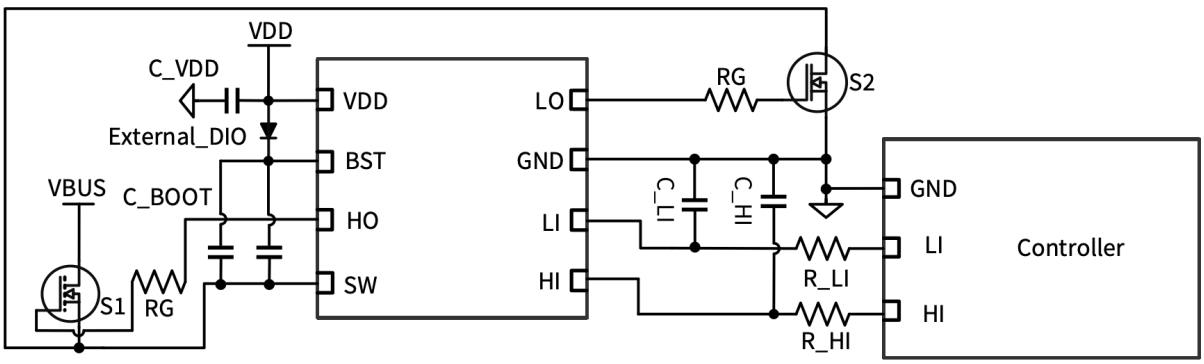

Figure 1 Simplified Half-Bridge Schematic

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2.Description of Design

2.1.Select Bootstrap and VDD Capacitor

The bootstrap capacitor must maintain the VHB(BST)-VHS(SW) voltage above the UVLO threshold for normal operation. Calculate the maximum allowable drop across the bootstrap capacitor, ΔVHB, with Equation 2-1.

$$\begin{aligned} \Delta VHB &= VDD - VDH - VHBL \\ \Delta VHB &= (6V - 1.1V - 3.8V) = 1.1V \end{aligned} \tag{2-1}$$

Where

- VDD is the supply voltage of gate driver device (Voltage=6V)
- VDH is the bootstrap diode forward voltage drop
- VHBL is the HB falling threshold ($V_{HB\_ON\_max}$-$VHB_{\_HYS}$)

In this example the allowed voltage drop across bootstrap capacitor is 1.1V.
Use Equation 2-2 to estimate the total charge needed per switching cycle from bootstrap capacitor.

$$\begin{aligned} Qtotal &= \mathrm{Qg} + I_{LK\_Q} * \frac{\mathrm{Dmax}}{f} + \frac{I_{BSTQ}}{f} \\ &= 44\mathrm{nC} + 0.001\mathrm{nC} + 0.8\mathrm{nC} = 44.801\mathrm{nC} \end{aligned} \tag{2-2}$$

Where

- Qg is the total MOSFET gate charge (CSD19532KTT)
- $I_{LK_Q}$is the BST to GND leakage current from datasheet
- Dmax is the converter maximum duty cycle
- f is operating frequency (500KHz)
- I_{BSTQ} is the BST quiescent current

The caculated total charge is 44.801nC.
Next, use Equation 2-3 to estimate the minimum bootstrap capacitor value.

$$C_{BOOT(min)} = \frac{\mathrm{Qtotal}}{\Delta VHB} = 40.73nF \tag{2-3}$$

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The calculated value of minimum bootstrap capacitor is 40.73nF. It should be noted that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than calculated value to allow for situations where the power stage may skip pulse due to various transient conditions. It is recommended to use a 100nF bootstrap capacitor in this example. It is also recommenced to include enough margin and place the bootstrap capacitor as close to the HB and HS pins as possible. Also place a small size, 0402, low value, 1000 pF, capacitor to filter high frequency noise, in parallel with main bypass capacitor.

For this application, choose a C_{BOOT} capacitor that has the following specifications: 0.1μF, 25 V, X7R. As a general rule the local VDD bypass capacitor must be greater than the value of bootstrap capacitor value. For this application choose a CVDD capacitor with the following specifications: 2.2μF, 25V, X7R C_{VDD} capacitor is placed across VDD and VSS pin of the gate driver. Similar to bootstrap capacitors, place a small size and low value capacitor in parallel with the main bypass capacitor. For this application, choose 0402,1000pF, capacitance in parallel with main bypass capacitor to filter high frequency noise. The bootstrap and bias capacitors must be ceramic types with X7R dielectric or better. Choose a capacitor with a voltage rating at least twice the maximum voltage that it will be exposed to. Choose this value because most ceramic capacitors lose significant capacitance when biased. This value also improves the long term reliability of the system.

2.2.Select External Gate Resistor

In high-frequency switching power supply applications where high-current gate drivers such as the NSD1224LA are used, parasitic inductances, parasitic capacitances and high-current loops can cause noise and ringing on the gate of power MOSFETs. Often external gate resistors are used to damp this ringing and noise. In some applications the gate charge, which is load on gate driver device, is significantly larger than gate driver peak output current capability. In such applications external gate resistors can limit the peak output current of the gate driver. it is recommended that there should be provision of external gate resistor whenever the layout or application permits.

Use Equation 2-4 to calculate the driver high-side source current.

$$I_{SRC\_HO} = \frac{\mathrm{VDD-VDH}}{R_{OHH}+R_G+R_{MOS}} \tag{2-4}$$

Where

- I_{SRC_HO} is the high-side, peak pull-up current
- R_{OHH} is the gate driver internal high-side pull-up resistor
- R_G is the external gate resistance connected between driver output and power MOSFET gate
- R_{MOS} is the MOSFET internal gate resistance provided by MOSFET datasheet

Use Equation 2-5 to calculate the driver high-side sink current.

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$$I_{SNK\_HO} = \frac{\text{VDD}-\text{VDH}}{R_{OHL}+R_G+R_{MOS}} \quad (2\text{-}5)$$

Where

- I_{SNK_HO} is the high-side, peak sink current
- R_{OHL} is the gate driver internal high-side pull-down resistor

Use Equation 2-6 to calculate the driver low-side source current.

$$I_{SRC\_LO} = \frac{\text{VDD}-\text{VDH}}{R_{OLH}+R_G+R_{MOS}} \quad (2\text{-}6)$$

Where

- I_{SRC_LO} is the low-side, peak source current
- R_{OLH} is the gate driver internal low-side pull-up resistor

Use Equation 2-7 to calculate the driver low-side sink current.

$$I_{SRC\_LO} = \frac{\text{VDD}-\text{VDH}}{R_{OLL}+R_G+R_{MOS}} \quad (2\text{-}7)$$

Where

- I_{SRC_LO} is the low-side, peak sink current
- R_{OLL} is the gate driver internal low-side pull-down resistor

Both high and low-side channels of the gate driver have a peak current rating of +3 A/-4A. These equations help reduce the peak current if needed. To establish different rise time value compared to fall time value, external gate resistor can be anti-paralleled with diode-resistor combination as shown in Figure 1. Generally selecting an optimal value or configuration of external gate resistor is an iterative process.

2.3.Estimate Driver Power Losses

The total power loss in gate driver device such as the NSD1224LA is the summation of the power loss in different functional blocks of the gate driver device. The main power consumption is composed of static power Losses and dynamic power Losses. This section will describe these two parts in detail.

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Use Equation 2-8 to calculate the total power losses

$$P_{tot} = P_{Q\_tot} + P_{SW\_tot} \tag{2-8}$$

Where

- P_{tot} is the total power losses
- P_{Q_tot} is the static power losses
- P_{SW_tot} is the dynamic power losses

Equation 2-9 describes how quiescent currents (I_{VDDQ} & I_{BSTQ}) and power supply voltage (VDD) affect the static power Losses

$$\begin{aligned} P_{Qtot} &= P_{QVDD} + P_{QBST} \\ &= (VDD * I_{VDDQ}) + (VDD - V_{DH}) * I_{BSTQ} \\ &= 6V * 0.4mA + (6V - 1.1V) * 0.4mA = 4.36mW \end{aligned} \tag{2-9}$$

Where

- VDD is the supply voltage of gate driver device (Voltage=6V)
- V_{DH} is the bootstrap diode forward voltage drop
- I_{VDDQ} and I_{BSTQ} are the quiescent currents

Equation 2-10 describes how MOSFETs gate charge (Qg) affects the dynamic losses,P_{SW_tot}.

$$\begin{aligned} P_{SW\_tot} &= 2 * VDD * Qg * f_{sw} * \frac{R_{AV}}{R_{AV}+R_G+R_{MOS}} \\ &= 2 * 6V * 44nC * 500K * 0.8 = 211.2mW \end{aligned} \tag{2-10}$$

Where

- Q_g is the total MOSFET gate charge
- R_{AV} is the average value of pullup and pulldown resistor

Assume there is 1Ω gate resistor in this example. The average value of maximum pullup and pulldown resistance of the driver output section is approximately 4.5 Ω. Substitute the application values to calculate the dynamic loss due to gate charge, which is 211.2mW here.

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2.4.Bootstrap Diode

The NSD1224LA incorporates the bootstrap diode necessary to generate the high-side bias for HO to work. The characteristics of this diode are important to achieve efficient, reliable operation. The device has a boot diode forward voltage drop rated at 0.5 V (TYP) and dynamic resistance of 2.5 Ω (TYP) for reliable charge transfer to the bootstrap capacitor. Due to process limitations, the charging efficiency of the internal bootstrap diode is much lower than that of the external Schottky diode, with a charging efficiency of about 50%. In applications where switching frequencies are very high or the loads are heavy, the device will heat seriously. In such applications it is necessary to use external Schottkey diode as bootstrap diode. Furthermore, when the low-side minimum pulse widths are very small, the diode peak forward current could be very high and peak reverse current could also be very high, specifically if high bootstrap capacitor value has been chosen. In order to reduce the diode peak current and high frequency interference of BST to SW supply voltage, it is recommended to use a large pulse width for charging BST voltage instead of a continuous narrow pulse width. As shown in Figure 2, it is recommended to select method 1 to pre-charge BST supply voltage. In addition, it is recommended to use two capacitors across BST and SW: a low capacitance ceramic surface-mount capacitor (such as 0603 1nF) for high frequency filtering placed very close to BST and SW pins, and another high capacitance value surface-mount capacitor for device bias requirements.

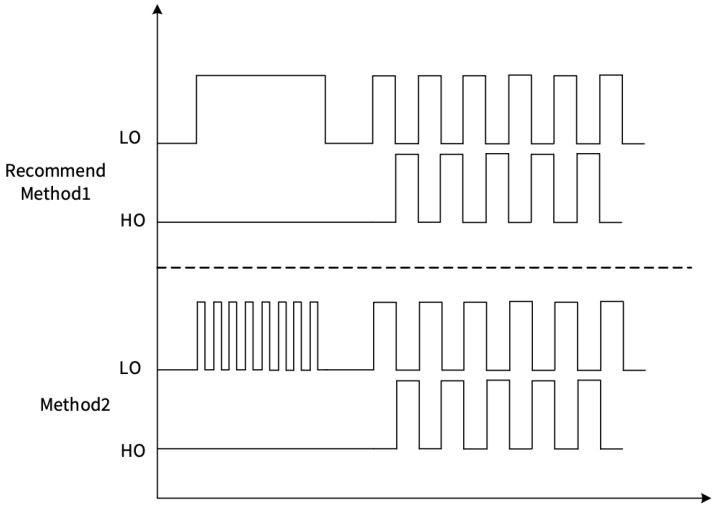

Figure 2 Starting Diagram

2.5.Input Filter

Some switching power supply applications are extremely noisy. Noise may come from ground bouncing and ringing at the inputs, (which are the HI and LI pins of the gate driver device). To mitigate such situations, the NSD1224LA offers both negative input voltage handling capability and wide input threshold hysteresis. If these features are not enough, then the application might need an input filter. Small filter such as 2.2Ω resistor and 47pF capacitor might be sufficient to filter noise at the inputs of the gate driver device. This RC filter would introduce delay and therefore need to be considered carefully. High frequency noise on bias supply can cause problems in performance of the gate driver device.

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3.Layout

3.1.Layout Guidelines

To achieve optimum performance of high-side and low-side gate drivers, one must consider following printed wiring board (PWB) layout guidelines.

Low ESR/ESL capacitors must be connected close to the device between VDD and GND pins and between HB and HS pins to support high peak currents drawn from VDD and HB pins during the turn-on of the external MOSFETs.

To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the high side MOSFET drain and ground (GND).

In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances between the source of the high-side MOSFET and the source of the low-side MOSFET (synchronous rectifier) must be minimized.

Overlapping of HS plane and ground (GND) plane should be minimized as much as possible so that coupling of switching noise into the ground plane is minimized.

Thermal pad should be connected to large heavy copper plane to improve the thermal performance of the device. Generally it is connected to the ground plane which is the same as VSS of the device. It is recommended to connect this pad to the VSS pin only.

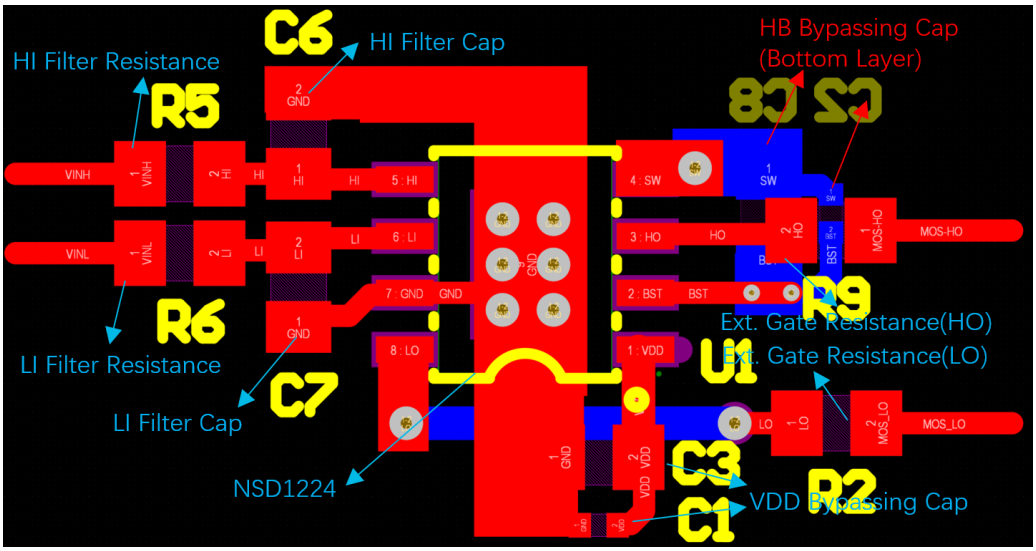

Figure 3 Starting Diagram

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4.Revision History

Revision	Description	Author	Date
1.0	Initial version	Xiangqian Li	2025/3/06

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